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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
BROCK II,P	
ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/277,893	MARR, KENNETH W.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-101* is/are pending in the application.

4a) Of the above claim(s) *1-16 and 34-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-33 and 50-101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 17 – 33 and 50 – 101 in Paper No. 8 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 83 and 89 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 83 recites the limitation "exposing selected regions of said layer of polysilicon". It is not clear how you can expose a layer of polysilicon. For the purposes of this office action "said layer of polysilicon" will be considered "said photoresist" in this claim.

Claim 89 recites the limitation "exposing selected regions of said layer of metal silicide". It is not clear how you can expose a layer of metal silicide. For the purposes of this office action "said layer of metal silicide" will be considered "said photoresist" in this claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17 and 19 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Sandhu.

Fischer et al. discloses a method of fabricating a fuse upon a semiconductor device in figures 1 – 3.

With regard to claim 17, In figure 1 Fischer et al. discloses disposing a layer of conductive material (11) over an insulative structure (10) of the semiconductor device. Fischer also discloses in figure 1 patterning the layer of conductive material to define at least two spaced apart regions of conductive material through which (111) the insulative structure is exposed. Fischer et al. discloses in figure 2 disposing a second conductive layer (12) over the semiconductor device, including adjacent to the at least two regions and to the insulative structure exposed between the at least two regions. In figure 3 Fischer et al. discloses patterning the second conductive layer so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two regions of conductive material, and a central region disposed between the at least two terminal regions and in contact with the insulative structure. Fischer et al. does not disclose the second conductive layer as a metal silicide. Sandhu teaches disposing a conductive layer of metal silicide in figure 1 and 2. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the metal silicide layer of Sandhu in the method of fabricating a fuse upon a semiconductor device of Fischer et al. in order to use the properties of low bulk resistance and low stress of the metal silicide as stated by Sandhu in column 1, lines 12 – 21.

With regard to claims 19, the method of Fischer et al. discloses in column 3, lines 42 - 50 patterning the layer of conductive material comprising disposing a mask over the semiconductor device and removing selected regions of the layer of conductive material through the mask.

With regard to claim 20, Fischer et al. does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto the semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al. in order to pattern the metal layer.

With regard to claims 21 and 22, the method of Fischer et al. discloses in column 3, lines 34 – 50 that the removing comprises isotropically etching the selected regions of the layer of conductive material through the mask.

With regard to claim 23, Fischer et al. does not disclose etching the selected regions of the layer of conductive material with a wet etch. It is well known in the art that etching can comprise wet etching the selected regions of the layer of conductive material. It would have been obvious to one of ordinary skill in the art to use the wet etching method in the process of Fishcer et al. in order to etch the conductive material with tapered edges.

With regard to claim 24, Fischer et al. discloses in column 2, lines 45 – 48 disposing the layer of conductive material comprises chemical vapor depositing the layer of conductive material.

With regard to claim 25 and 26, Fischer et al. in view of Sandhu discloses in figure 1 of Sandhu that depositing the layer of metal silicide (12) comprises chemical vapor depositing the layer of metal silicide. Sandhu also discloses the metal silicide is tungsten silicide.

With regard to claim 27, the method of Fischer et al. in view of Sandhu inherently discloses patterning the layer of metal silicide comprising disposing a mask over the semiconductor device and removing selected regions of the layer of metal silicide through the mask.

With regard to claim 28, Fischer et al. in view of Sandhu does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto the semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al. in view of Sandhu in order to pattern the metal silicide.

With regard to claims 29 and 30, the method of Fischer et al. in view of Sadhu inherently discloses that the removing comprises anisotropically etching the selected regions of the layer of metal silicide.

With regard to claim 31, Fischer et al. does not disclose etching the selected regions of the layer of the metal silicide with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions of the layer of metal silicide. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Fischer et al. in view of Sandhu in order to etch the metal silicide with vertical edges.

With regard to claim 32, it is inherent that a contact is disposed in communication with at least one of the at least two terminal regions.

With regard to claim 33, it is inherent that another contact is disposed in communication with another of the at least two terminal regions.

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Sandhu as applied to claim 17 above, and further in view of Szluk et al.

With regard to claim 18, Fischer et al. does not disclose that disposing the layer of the conductive material comprises disposing polysilicon onto the insulative structure. Szluk et al. discloses disposing polysilicon (22) as a conductive material for a fuse structure (50) in figures 1 – 5. It would have been obvious to one of ordinary skill in the art at the time of the present invention to dispose the polysilicon of Szluk et al. in the method of Fischer et al. in order to dispose a conductive material layer that will be both part of the fuse component and a gate electrode as stated by Szluk et al. in column 2, lines 39 – 43.

7. Claims 50, 51, and 55 – 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Sandhu, and further in view of Szluk et al.

With regard to claim 50, Fischer et al. discloses in figures 1 – 3 a method of fabricating a fuse. Fischer et al. discloses in figure 1 fabricating spaced (111) apart regions comprising a first conductive layer (11) on an insulative structure (10) of a semiconductor device. Fischer et al. discloses in figures 2 and 3 fabricating a fuse comprising a second conductive layer (12), including a central region disposed adjacent the insulative structure and between the spaced apart regions and at least two terminal regions disposed on opposite ends of the central region and adjacent the space apart regions. Fischer et al. does not disclose that the first conductive layer comprises polysilicon on the insulative structure. Szluk et al. discloses polysilicon (22) as a conductive layer for a fuse structure (50) in figures 1 – 5. It would have been obvious to one of ordinary skill in the art at the time of the present invention to dispose the polysilicon of Szluk et al. in the method of Fischer et al. in order to use a first conductive layer that will be both part of

the fuse component and a gate electrode as stated by Szluk et al. in column 2, lines 39 – 43. Fischer et al. does not disclose the second conductive layer as a metal silicide. Sandhu teaches a conductive layer of metal silicide in figure 1 and 2. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the metal silicide layer of Sandhu in the method of fabricating a fuse upon a semiconductor device of Fischer et al. in order to use the properties of low bulk resistance and low stress of the metal silicide as stated by Sandhu in column 1, lines 12 – 21.

With regard to claim 51, Fischer et al. discloses in figure 1 disposing the first conductive layer onto the insulative structure, and patterning the conductive material. As applied above the first conductive layer is polysilicon.

With regard to claims 55, the method of Fischer et al. discloses in column 3, lines 42 – 50 patterning comprises disposing a mask adjacent the first conductive layer and removing selected regions of the conductive layer through the mask. As applied above the first conductive layer is polysilicon.

With regard to claim 56, Fischer et al. does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist adjacent the first conductive layer, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al. in order to pattern the first conductive layer. As applied above the first conductive layer is polysilicon.

With regard to claims 57 and 58, the method of Fischer et al. discloses in column 3, lines 34 – 50 that the removing comprises isotropically etching the selected regions of the first conductive layer through the mask. As applied above the first conductive layer is polysilicon.

With regard to claim 59, Fischer et al. does not disclose etching the selected regions of the first conductive layer with a wet etch. It is well known in the art that etching can comprise wet etching the selected regions first conductive layer. It would have been obvious to one of ordinary skill in the art to use the wet etching method in the process of Fishcer et al. in order to etch the first conductive layer with tapered edges. As applied above the first conductive layer is polysilicon.

With regard to claim 60, Fischer et al. discloses in figure 2 disposing the second conductive layer adjacent the spaced apart regions and the insulative structure exposed therebetween. As applied above the second conductive layer is a metal silicide.

With regard to claim 61 and 62, Fischer et al. in view of Sandhu discloses in figure 1 of Sandhu that depositing the layer of metal silicide (12) comprises chemical vapor depositing the layer of metal silicide. Sandhu also discloses the metal silicide is tungsten silicide.

With regard to claim 63, the method of Fischer et al. in view of Sandhu inherently discloses patterning the layer of metal silicide comprising disposing a mask over the semiconductor device and removing selected regions of the layer of metal silicide through the mask.

With regard to claim 64, Fischer et al. in view of Sandhu does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto the semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would

have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al. in view of Sandhu in order to pattern the metal silicide.

With regard to claims 65 and 66, the method of Fischer et al. in view of Sadhu inherently discloses that the removing comprises anisotropically etching the selected regions of the metal silicide.

With regard to claim 67, Fischer et al. does not disclose etching the selected regions of the layer of the second conductive layer with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions of the layer of second conductive layer. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Fischer et al. in view of Sandhu in order to etch the metal silicide (as applied above the second conductive layer is metal silicide) with vertical edges.

With regard to claim 68, Fischer et al. discloses in figures 2 and 3 the patterning of the second conductive layer comprises defining the at least two terminal regions of the fuse adjacent the spaced apart regions and the central region of the fuse adjacent the insulative structure. As applied above the second conductive layer is metal silicide.

8. Claims 52 – 54, 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Sandhu, and further in view of Szluk et al. as applied to claims 50 and 51 above, and further in view of Degelormo et al.

Fischer et al. in view of Sandhu, and further in view of Szluk et al. does not disclose disposing the polysilicon by chemical vapor deposition. Degelormo et al. teaches in column 6, lines 60-63 of chemical vapor depositing doped polysilicon wherein doping occurs substantially

simultaneously with the disposing. The method of Degelormo et al. would further allow the spaced apart regions of polysilicon to be doped, and the doping to occur substantially simultaneously with disposing polysilicon on the insulative structure. It would have been obvious to use the polysilicon disposing method of Degelormo et al. in the method of Fischer et al. in view of Sandhu, and further in view of Szluk et al. in order to make lower resistance polysilicon as stated by Degelormo et al. in column 6, lines 32 – 35.

9. Claims 71, 80 – 86, 88 – 92 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Szluk et al. in view of Bohr et al.

With regard to claim 71, Szluk et al. discloses in figures 1 – 5 a method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate. Szluk et al. in figure 1 disposes a layer of insulative material (26, 24) over at least an exposed region of the semiconductor substrate (13). Szluk et al. in figure 1 also disposes a layer of polysilicon (22, 23) over the semiconductor substrate, including over the layer of insulative material and over field oxide regions (14) disposed on the semiconductor substrate. Szluk et al. further discloses in figure 1 patterning at least regions of the layer of polysilicon (22) disposed over at least one field oxide region of the field oxide regions. Szluk et al. does not disclose forming a layer of metal silicide on the layer of polysilicon. Bohr et al. teaches in figure 1a and 1b and column 3, lines 6 – 14 disposing a layer of metal silicide on a layer of polysilicon and patterning at least the layer of metal silicide to define the fuse and the gate therefrom. It would have been obvious to use the metal silicide layer and patterning of Bohr et al. in the method of Szluk et al. in order to form the polysilicon and silicide layer of the fuse device by the same processing steps used to produce the polysilicon and silicide gate layers as stated by Bohr et al. in column 3, lines 7 – 11.

With regard to claims 80 and 81, Szluk et al. discloses in figure 1 patterning gate regions of the layer of polysilicon. It is inherent that the patterning the gate regions occurs substantially simultaneously with the patterning the at least regions of the layer of polysilicon.

With regard to claim 82, the method of Szluk et al. inherently comprises disposing a mask over the layer of polysilicon and removing selected regions of the layer of polysilicon through the mask.

With regard to claim 83, Szluk et al. does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto a semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Szluk et al. in order to pattern the polysilicon.

With regard to claims 84 and 86, the method of Szluk et al. inherently discloses that the removing comprises anisotropically etching the selected regions.

With regard to claim 85, Szluk et al. does not disclose etching the selected regions with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Szluk et al. in order to etch the polysilicon to have vertical sidewalls.

With regard to claim 88, the method of Szluk et al. in view of Bohr et al. defining the gate from at least the layer of metal silicide inherently comprises disposing a mask over the layer of metal silicide and removing selected regions of the layer of metal silicide through the mask.

With regard to claim 89, Szluk et al. in view of Bohr et al. does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask over a layer of metal

silicide, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Szluk et al. in view of Bohr et al. in order to pattern the metal silicide.

With regard to claims 90 and 92, the method of Szluk et al. in view of Bohr et al. inherently discloses that the removing comprises anisotropically etching the selected regions.

With regard to claim 91, Szluk et al. in view of Bohr et al. does not disclose etching the selected regions with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Szluk et al. in view of Bohr et al. in order to etch the metal silicide to have vertical sidewalls.

With regard to claim 101, Szluk et al. discloses in figure 1 doping at least one source region (18) and at least one drain region (19) of the semiconductor substrate, the at least one source region and the at least one drain region disposable adjacent the gate on opposite sides thereof.

10. Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Szluk et al. in view of Bohr et al. as applied to claim 71 above, and further in view of Degelormo et al.

Szluk et al. in view of Bohr et al. does not disclose disposing the polysilicon by chemical vapor deposition. Degelormo et al. teaches in column 6, lines 60-63 of chemical vapor depositing doped polysilicon. It would have been obvious to use the polysilicon disposing method of Degelormo et al. in the method of Szluk et al in view of Bohr et al. in order to make lower resistance polysilicon as stated by Degelormo et al. in column 6, lines 32 – 35.

11. Claims 73 – 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Szluk et al. in view of Bohr et al. as applied to claim 71 above, and further in view of Fischer et al.

With regard to claims 73 and 74, the method of Szluk et al. in view of Bohr et al. does not disclose defining at least two spaced apart regions of polysilicon. Fischer et al. teaches in figure 1 patterning regions (11) comprising defining at least two spaced apart regions of a conductor layer on the at least one field oxide region (10) and between which a portion of the at least one field oxide region is exposed. Fischer et al. also teaches in figure 2 and 3 defining a fuse comprising defining a central region (111) disposed adjacent and substantially between the at least two spaced apart regions and defining at least two terminal regions, each terminal region continuos with an end of the central region and disposed adjacent one of the at least two spaced apart regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to pattern the silicon layer of Szluk et al. with the two spaced apart regions of Fischer et al. in order to create a laser-programmable or electric-current-programmable link features having locally reduced cross-sectional area resulting from locally reduced thickness of a conductive path, while width remains essentially constant, as stated by Fischer et al. in column 1, lines 60 – 65.

With regard to claim 75, the method of Szluk et al. in view of Bohr et al. and further in view of Fischer et al. defining the at least two spaced apart regions inherently comprises disposing a mask over the layer of polysilicon and removing selected regions of the layer of polysilicon through the mask.

With regard to claim 76, Szluk et al. in view of Bohr et al. and further in view of Fischer et al. does not disclose that the mask is photoresist. It is well known in the art to dispose a

photoresist mask over a layer of polysilicon, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Szluk et al. in view of Bohr et al. and further in view of Fischer et al. in order to pattern the polysilicon.

With regard to claims 77 and 79, the method of Szluk et al. in view of Bohr et al. and further in view of Fischer et al. inherently discloses that the removing comprises isotropically etching the polysilicon.

With regard to claim 78, Szluk et al. in view of Bohr et al. does not disclose etching the selected regions with a wet etch. It is well known in the art that etching can comprise wet etching the selected regions of polysilicon. It would have been obvious to one of ordinary skill in the art to use the wet etching method in the process of Szluk et al. in view of Bohr et al. and further in view of Fischer et al. in order to etch the polysilicon to have slanted side walls.

12. Claim 87 is rejected under 35 U.S.C. 103(a) as being unpatentable over Szluk et al. in view of Bohr et al. as applied to claim 71 above, and further in view of Sandhu.

Szluk et al. in view of Bohr et al. does not disclose disposing metal silicide by chemical vapor deposition. Sandhu teaches in figure 1 disposing a layer of metal silicide comprising chemical vapor depositing the layer of metal silicide (12). It would have been obvious at the time of the present invention to use the disposing of metal silicide method of Sandhu in the method of Szluk et al. in view of Bohr et al. in order to use the properties of low bulk resistance and low stress of the metal silicide as stated by Sandhu in column 1, lines 12 – 21.

13. Claims 93 – 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Szluk et al. in view of Bohr et al. as applied to claim 71 above, and further in view of Ukeda et al.

Szluk et al. in view of Bohr et al. do not disclose removing exposed regions of polysilicon through the layer of metal silicide or removing exposed regions of the insulative material through the layer of polysilicon. Ukeda et al. discloses in figures 1f and 1g and columns 3 and 4, lines 64 – 67 and 1 – 15 respectively removing exposed regions of polysilicon (3) through a layer of metal silicide (7) by anisotropically, dry etching the exposed regions. Ukeda et al. also discloses in figures 1f and 1g and columns 3 and 4, lines 64 – 67 and 1 – 15 respectively removing exposed regions of the layer of insulative material (2) through the layer of polysilicon by anisotropically, dry etching the exposed regions of insulative material. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the removing methods of Ukeda et al. in the method of Szluk et al. in view of Bohr et al. in order to complete the formation of a transistor furnished with a gate electrode as described by Ukeda et al. in column 4, lines 10 – 15.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Park et al teaches forming a fuse with two spaced apart regions of a conductive material whereby another conductive material overlies the insulative material between the spaced apart regions. Peyre-Lavigne et al, Froehner, Sur, Jr. et al., Bryant et al., Makai, Price, and Ramachandra et al. all disclose methods of making a fuse.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
December 19, 2000

Jerome Jackson, Jr.
Primary Examiner